CURRICULUM VITAE

YOUNGSOO SHIN

School of Electrical Engineering
KAIST

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EDUCATION:

- B.S., M.S., Ph.D. Electronics Engineering Seoul National University Feb. 2000

WORK EXPERIENCE:

- 3/2021 – present: ***KAIST ICT Endowed Chair Professor***, KAIST, Daejeon, Korea
- 3/2018 – present: ***Independent Director***, LX Semicon (formerly Silicon Works), Seoul, Korea
- 1/2016 – present: ***CTO***, ***Co-CEO***, Baum, Seoul, Korea
- 7/2004 – present: ***Assistant Professor, Associate Professor, Professor***, School of EE, KAIST, Daejeon, Korea
- 2/2011 – 2/2014: ***Consulting Professor***, LG Electronics, Seoul, Korea
- 8/2001 – 6/2004: ***Research Staff Member***, IBM T. J. Watson Research Center, Yorktown Heights, NY, USA
- 3/2000 – 8/2001: ***Research Associate***, University of Tokyo, Tokyo, Japan

RESEARCH INTERESTS:

- VLSI CAD of integrated circuits and systems
- Low-power/low-leakage design & design methodology, thermal analysis and design, NTV design
- Latch-based circuit
- Logic synthesis, timing analysis, sequential synthesis
- DFM (design for manufacturability), computational lithography, DSA (directed self assembly)
- AI circuit (Processing-in Memory), DNA circuit
- Publications: http://dtlab.kaist.ac.kr

AWARDS AND HONORS:

SOCIETY AWARDS

- ***IEEE CEDA Outstanding Service Recognition,*** 2019
- ***IEEE Fellow,*** 2017 (for contributions to design tools for low power, high speed VLSI circuits and systems)
- ***ACM Senior Member,*** 2013

INTERNATIONAL

- ***Invitation Fellowship for Research in Japan,*** Japan Society for the Promotion of Science, 2016
- ***IP Excellence Award***, 4th LSI IP Design Award, Japan, 2002

PAPER AWARDS AND AWARD NOMINATIONS

- ***Best Paper Award – Honorable Mention,*** IEEE Trans. on Semiconductor Manufacturing (TSM), 2022
- ***Best Paper Award,*** IEEE Trans. on Semiconductor Manufacturing (TSM), 2021
- ***Nominated for Best Paper Award,*** Great Lakes Symposium on VLSI (GLSVLSI), 2020
- ***Nominated for Best Paper Award,*** Asia-South Pacific Design Automation Conf., 2020
- ***Best Paper Award,*** Int'l SoC Design Conf. (ISOCC), 2015
- ***Nominated for Best Paper Award,*** Int'l Symp. on Quality Electronic Design (ISQED), 2007
- ***Best Paper Award,*** Int'l SoC Design Conf. (ISOCC), 2006
- ***Best Paper Award,*** Int'l Symp. on Quality Electronic Design (ISQED), 2005

FROM UNIVERSITY

- ***KAIST ICT Endowed Chair Professor,*** KAIST, 2021
- ***Technology Innovation Award,*** College of Engineering, KAIST, 2020
- ***Department Faculty Teaching Award,*** Dept. of EE, KAIST, spring semester, 2018
- ***Department Faculty Teaching Award,*** Dept. of EE, KAIST, fall semester, 2016
- ***Department Faculty Teaching Award,*** Dept. of EE, KAIST, fall semester, 2012
- ***Department Faculty Teaching Award,*** Dept. of EE, KAIST, spring semester, 2008

PROFESSIONAL ACTIVITIES:

JOURNAL EDITORSHIP

- ***Associate Editor*** (2016 – 2018), IEEE Design & Test
- ***Associate Editor*** (2012 – 2017), IEEE Trans. on CAD (TCAD)
- ***Associate Editor*** (2011–2014), ACM Trans. on Design Automation of Electronic Systems (TODAES)
- ***Best Paper Selection Committee*** (2014), ACM Trans. on Design Automation of Electronic Systems (TODAES)
- ***TCAD Advisory Committee*** (2014), IEEE Trans. on CAD (TCAD)

CONFERENCE ORGANIZATION ACTIVITIES

- ***General Chair*** (2018), Asia-South Pacific Design Automation Conf. (ASP-DAC)
- ***TPC Chair*** (2015), IFIP/IEEE Int'l Conf. on Very Large Scale Integration (VLSI-SoC)
- ***TPC Chair*** (2014), Int'l Conf. on Computer Design (ICCD)
- ***Steering Committee***, Asia-South Pacific Design Automation Conf. (ASP-DAC), as *ICCAD Representative* (2013-2015), as *ASP-DAC 2018 GC* (2019), as *International Members* (2021-)
- ***Best Paper Selection Committee*** (2018), Int'l Conf. on CAD (ICCAD)
- ***Executive Committee***, Int'l Conf. on CAD (ICCAD), as *Asian Representative* (2013-2015)
- ***Finance Chair*** (2012), Int'l Conf. on Field-Programmable Technology (FPT)
- ***TPC Secretary*** (2011), Asia-South Pacific Design Automation Conf. (ASP-DAC)
- ***Special Session Chair*** (2017), IFIP/IEEE Int'l Conf. on Very Large Scale Integration (VLSI-SoC)
- ***Special Session Chair*** (2011), Int'l Symp. on Low-Power Electronics and Design (ISLPED)
- ***General Secretary*** (2008), Asia-South Pacific Design Automation Conf. (ASP-DAC)
- ***Industry Liaison*** (2006), Int'l Conf. on Compilers, Architecture, and Synthesis for Embedded Systems (CASES)
- ***Tutorial Chair*** (2019), Int'l Conf. on Artificial Intelligence Circuits and Systems (AICAS)
- ***Tutorial Chair*** (2007, 2008), Int'l SoC Design Conf. (ISOCC)
- ***Track Chair***, *EDA6. Digital Design, Timing and Simulation* (2020, 2021), Design Automation Conf. (DAC)
- ***Track Chair***, *Physical Design & 3D Integration* (2014), IFIP/IEEE Int'l Conf. on Very Large Scale Integration (VLSI-SoC)
- ***Track Chair***, *Signal/Power Integrity, Interconnect/Device/Circuit Modeling and Simulation* (2012), Asia-South Pacific Design Automation Conf. (ASP-DAC)

  Track Chair (2010) and ***Vice-Chair*** (2011), *Design Tools*, Int'l Symp. on Low-Power Electronics and Design (ISLPED)
- ***Track Chair***, *Timing, Power, Thermal Analysis and Optimization* (2008, 2009, 2010), Asia-South Pacific Design Automation Conf. (ASP-DAC)
- ***Track Chair***, *Trends and Perspective in Architecture and System-Level Design* (2004), Int'l Conf. on CAD (ICCAD)
- ***Session Chairs/Organizers***, DAC (2023, 2011), ICCAD (2015, 2012, 2008, 2005), ASP-DAC (2013, 2012, 2011, 2009, 2008, 2007, 2006), ISLPED (2011, 2004), CASES (2006)
- ***Organizer,*** International Workshop on IT and Future Society (hosted by IDEC, KAIST), Jeju Island (2010, 2011)

CONFERENCE TECHNICAL PROGRAM COMMITTEES

- Design Automation Conf. (DAC), 2009-2010, 2014-2015, 2020-2021
- Int'l Conf. on CAD (ICCAD), 2003-2005, 2015, 2019
- Asia-South Pacific Design Automation Conf. (ASP-DAC), 2005-2010, 2012, 2014
- Design, Automation and Test in Europe Conf. (DATE), 2022

- Int'l Symp. on Low-Power Electronics and Design (ISLPED), 2003-2011
- SIGDA Ph.D. Forum at DAC, 2005-2011
- Int'l Symp. on Circuits and Systems (ISCAS), 2006
- Asia Symp. on Quality Electronic Design (ASQED), 2009, 2011
- IEEE Computer Society Annual Symp. on VLSI (ISVLSI), 2009
- Int'l Conf. on ASIC (ASICON), 2005
- Int'l Conf. on Embedded Software and Systems (ICESS), 2005
- Int'l Workshop on Advanced Low Power Systems, 2006

TECHNICAL SOCIETY ACTIVITIES

- *(Founding) Chair,* ACM SIGDA Korea Chapter, 2014
- *Review Board,* National Research Foundation (NRF) of Korea, 2018.11 – 2021.10
- *Member-at-Large*, ACM SIGDA Low-Power Technical Committee (LPTC), 2010 – present
- *Society Membership*, IEEE (Fellow), ACM/ACM SIGDA (Senior Member), IEEK (Life Member)

INVITED TALKS (RECENT)

1. "Lightening Talk: EDA with ML, Rule-Based, or Both?" *Design Automation Conference (DAC)*, San Francisco, USA, July 12, 2023.
2. "Reshaping EDA with Machine Learning," *Cadence Tech Talk*, Virtual, August 27, 2021.
3. "Machine Learning Models for EDA Applications," 34th Symp. on Integrated Circuits and Systems Design (SBCCI), Virtual, August 25, 2021.
4. "Computational Lithography Using Machine Learning Models," invited short course at *Next Generation Lithography Conference*, Virtual, June 25, 2021.
5. "Machine Learning Models for EDA Applications," Synopsys, Virtual, June 24, 2021.
6. "Computational Lithography Using Machine Learning Models," invited short course at *Next Generation Lithography Conference*, Virtual, November 18, 2020.
7. "Lithography Optimization through Machine Learning," invited short course at *Next Generation Lithography Conference*, Incheon, Korea, August 21, 2019.
8. "Low Power Design: Facts, Myths, and Misunderstandings," special invited lecture at *IEEE Symposium on Low-Power and High-Speed Chips and Systems (COOL Chips 22)*, Yokohama, Japan, April 17, 2019.
9. "Lithography Optimizations through Machine Learning," *11th IEEE/ACM Workshop on Variability Modeling and Characterization* (at ICCAD), San Diego, USA, Nov. 8, 2018.
10. "Lithography Optimizations through Machine Learning," Nagoya University, Nagoya, Japan, Oct. 5, 2018.
11. "Machine Learning for SoC Design and Manufacturing," Samsung Advanced Institute of Technology, Suwon, Korea, July 6, 2018.

12. "Machine Learning for IC Design and Manufacturing," KAIST-DKU Intelligent Technology Innovation Forum (at Duke-Kunshan University), China, June 20, 2018.
13. "Machine Learning for SoC Design and Manufacturing," SoC Conference (at Sungkyunkwan University), Suwon, Korea, May 11, 2018.
14. "Physical Design Optimization for Directed Self-Assembly Lithography," Tokyo Institute of Technology, Tokyo, Japan, Feb 14, 2017.
15. "Exploring Sequencing Elements to Optimize ASIC/SoC Designs," Osaka University, Osaka, Japan, Feb 10, 2017.
16. "Directed Self-Assembly Lithography (DSAL): Mask Synthesis and Circuit Design," tutorial at *Asia South Pacific Design Automation Conf. (ASP-DAC)*, Jan 25, 2016, Macao.
17. "Physical Synthesis for DFM," Samsung Electronics, Hwasung, Korea, July 9, 2015.